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1	3632	716/\$.ccls.	USPAT	2003/02/04 13:51
2	500	((716/12) or (716/13) or (716/14)).CCLS.	USPAT	2003/02/04 13:54
3	10	((((716/12) or (716/13) or (716/14)).CCLS.) and linear near3 (program\$4 or problem)	USPAT	2003/02/04 14:02
4	9765	net and partition\$3 snf rout\$3 and linear near2 program\$4 and edge	USPAT	2003/02/04 14:05
5	461	716/\$.ccls. and (net and partition\$3 snf rout\$3 and linear near2 program\$4 and edge)	USPAT	2003/02/04 14:05
6	92	((((716/12) or (716/13) or (716/14)).CCLS.) and (net and partition\$3 snf rout\$3 and linear near2 program\$4 and edge)	USPAT	2003/02/04 14:05
7	90	(((((716/12) or (716/13) or (716/14)).CCLS.) and (net and partition\$3 snf rout\$3 and linear near2 program\$4 and edge)) not (((((716/12) or (716/13) or (716/14)).CCLS.) and linear near3 (program\$4 or problem)))	USPAT	2003/02/04 14:41
8	326	(716/12).CCLS.	USPAT	2003/02/04 14:41
9	2	((716/12).CCLS.) and (partition\$3 with region)	USPAT	2003/02/04 14:42
10	4	((716/12).CCLS.) and (linear near3 (program\$3 or problem))	USPAT	2003/02/04 14:44
11	2	partition\$3 same net same edge same rout\$3	USPAT	2003/02/04 14:47

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**Four-bend top-down global routing**

Cho, J.D. Sarrafzadeh, M.

Sch. of Electr. &amp; Comput. Eng., Sungkyunkwan Univ., Suwon;

*This paper appears in: Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*

On page(s): 793-802

Volume: 17, Sep 1998

ISSN: 0278-0070

References Cited: 31

CODEN: ITCSDI

INSPEC Accession Number: 6041727

**Abstract:**

We propose a new global net distribution approach for high-performance  $m \times m$  two-dimensional arrays of very large scale integration and multichip-modules. The objective is to route  $n$  nets with minimum density of global cells, using a small number of bends. There are a number of applications where it is necessary to limit the number of bends on each wire. For example, it is desired to limit the number of bends on each microstrip (transmission) line, for mismatch of line impedance can cause reflections from the junction points such as bends and vias. Furthermore, for high-performance routing, intersections of wires cause the use of more vias, which in turn require the use of more routing resources (because of the larger via pitch). This is the first paper that addresses a graph-theoretic framework to solve the bend-constrained global routing problem in two-dimensional arrays. In this paper, at each level of an underlying quad-tree, we present a four-bend routing algorithm by decomposing the original problem at level  $i$  into subproblems that can be solved exactly based on a two-stage approach of smaller-sized linear program followed by min-cost flow networks. The overall (entire level of the four-way partition hierarchy) constraint and variable size for the first stage is  $O(m d_0)$ , while the overall run time for the second stage is  $O(n^3 \log n^2)$ . The time complexity of such a hierarchical approach is one order of magnitude less than one of constructing a global routing using the min-cost-flow-based flow design approach. Last, we present an extension that permits a limited degree control over the number of bends. The proposed algorithm can also be used for estimating the wireability in the early design planning stage for high-level synthesis. Experimental results showed the effectiveness of the proposed algorithm.

**Index Terms:**

VLSI circuit layout CAD computational complexity flow graphs high level synthesis integrated circuit layout linear programming logic partitioning network routing wiring

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